Lab 7

Sequential Circuits(State Machines)

RTL Modeling

Learning objective of this lab

* Describing state machine as three separate components; Next State Logic, Present State and Output Logic.
* Naming constants using parameter, so that they are more understandable.
* Generating Clock signal in testbench.
* Pre-Lab
  1. Introduction

A synchronous circuit consists of two kinds of elements: registers and combinational logic. Figure 7.1 shows the generic form of a sequential circuit. The brown colored signal depends on the type of machine. It is only present for a Mealy-type circuit. For a Moore-type circuit, it is absent.

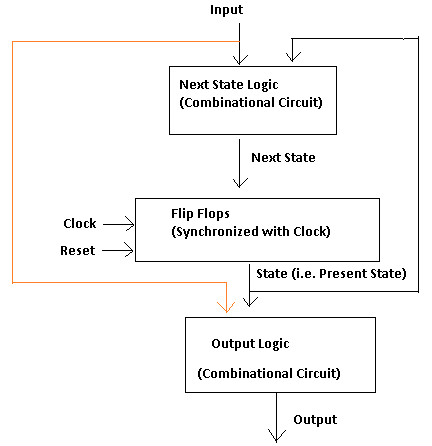


Figure 8.1 (The Colored wire is there only in Mealy Machines. For Moore Machines Remove it)

* 1. Hardware Description
     1. Combinational Part

The two combinational circuits (Next State Logic & Output Logic) can be described using any of the techniques studied in earlier labs i.e. gate level modeling, continuous assignment or procedural assignment inside cyclic behaviors (always @). Recommended method is cyclic behaviors.

* + 1. Sequential Part

The clocked part of the circuit is described using RTL modeling inside cyclic behaviors. It is almost similar to the topic studied in the previous lab. The differences are

* Inside the sensitivity list @ posedge clock is used. It means that the assignments written inside the cyclic behavior will only execute when clock changes from 0 to 1

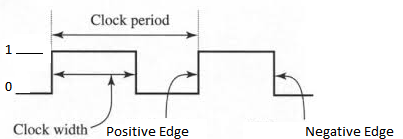
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Figure 7.2(Clock Signal)

* Non-Blocking assignment operator (<=) is used. All the assignments written using <= execute in parallel so the order in which they are listed has no effect.

For example, if a=1, b=2, c=3

b=c

a=b will result in a=c=3

but

b<=c

a<=b will result in b=3, a=2

* Reset signal is compulsory for the sequential part and there are different modes of reset
  + Synchronous Reset (Synchronized with clock)

always @ ( posedge clk)

begin

if(reset)

//reset the Flipflops

else

//do required task

end

* + Asynchronous Reset
    - Edge Triggered Reset

always @ ( posedge clk or negedge reset)

begin

if(reset==0)

//reset the Flipflops

else

//do required task

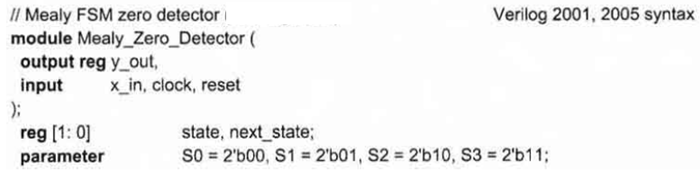
end

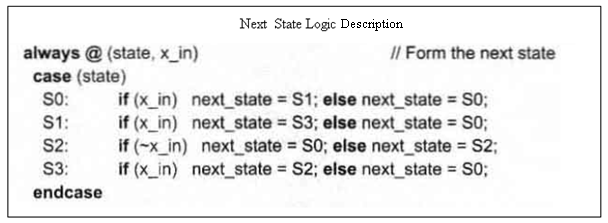
* In-Lab
  1. Code Example

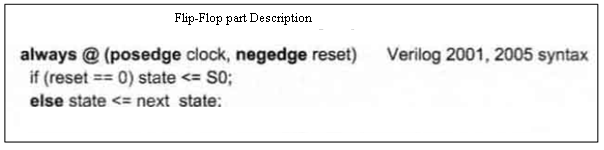
Given below is the state diagram of a Mealy Machine

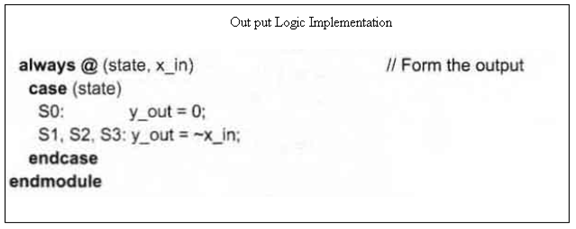


Figure 7.3









* 1. Clock Generators for Testbench

Clock generators are used in testbenches to provide a clock signal for testing the model of a synchronous circuit. The forever loop causes unconditional repetitive execution of statements, subject to the disable statement, and is a convenient construct for describing clocks. You will have to add the following two single-pass behaviors to your testbench to generate clock signal.

reg clock;

parameter half\_cycle = 50;

parameter stop\_time = 350;

initial

begin: give\_any\_name // Note: give\_any\_namme is a named block of //statements

clock = 0;

forever

begin

#half\_cycle clock = 1;

#half\_cycle clock = 0;

end

end

initial

#stop\_time disable give\_any\_name;

**Task (Each Task given below is a combination of Mealy and Moore. So you should write two output behaviors (combinational) for each task. One for Mealy ouputs and the other for Moore.**

* **Figure given below shows a numpad. When a key is pressed the connected line is set to 1, otherwise all the lines are at level 0. For example if 7 is pressed A=1 and E=1. Write the HDL description of its controller described by the state machine given**

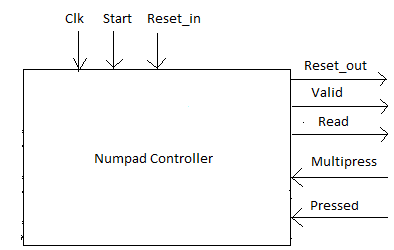
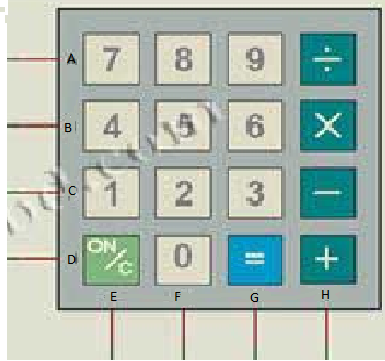
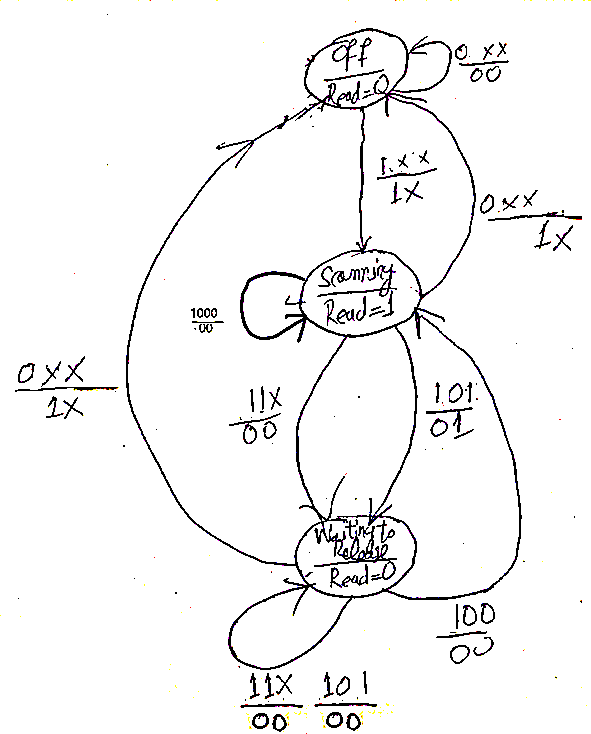
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Figure Task1a Figure Task 1b

The Labeling on state transition arrows e.g. 11x/x, is **input vector/Mealy output vector**. The input vector written on the State Diagram is {Start, Multi\_press, Pressed}. Mealy output is {Reset\_out, Valid}.

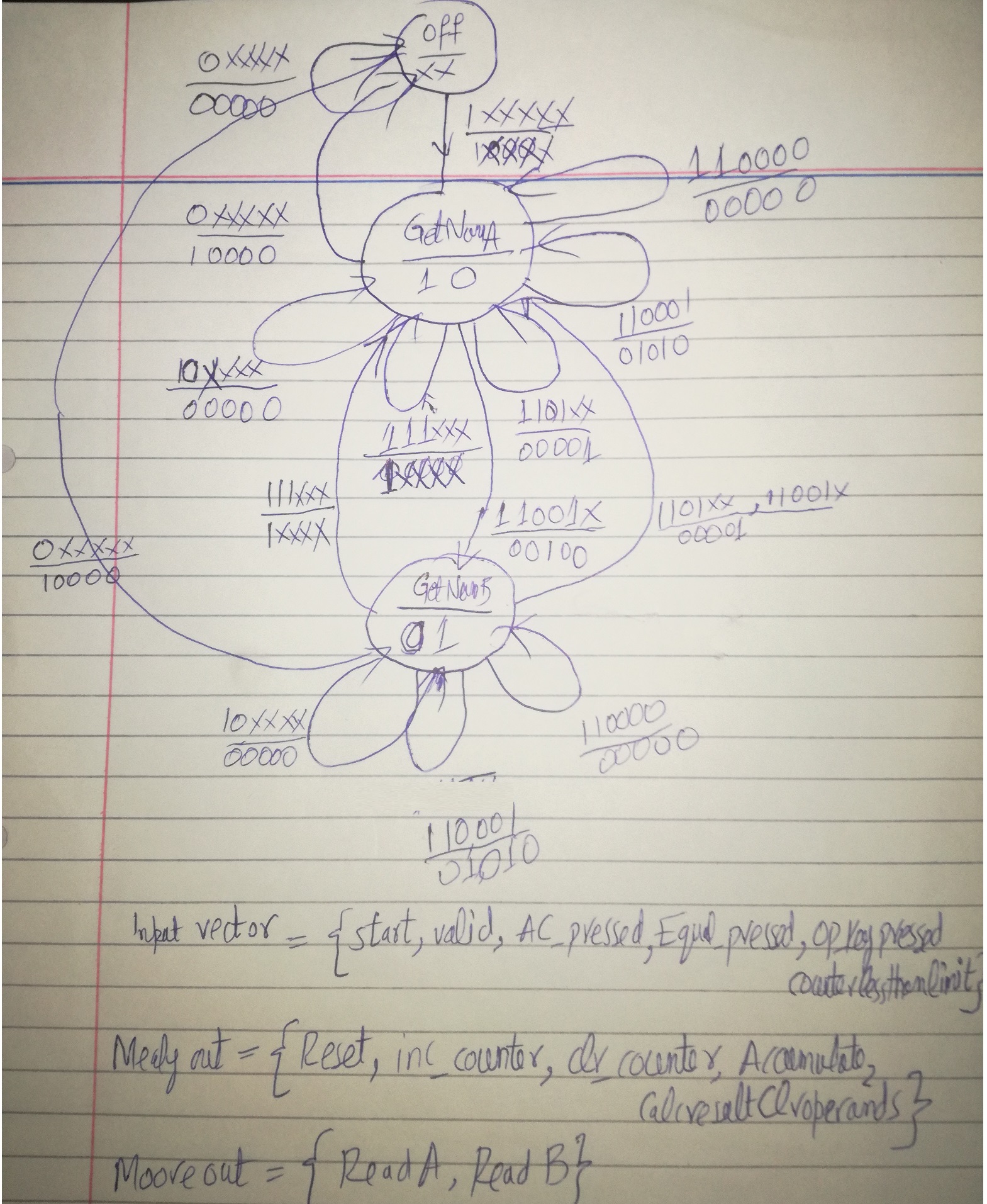
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**Figure 1b (State Diagram)**

* Post-Lab
* **Write the HDL description of controller of a calculater. Its state Diagram is given below. The input vector= { start, valid, AC\_pressed, Equal\_pressed, OpKey\_pressed, counterlessthanlimit}**

**Moore Ouput Vector ={ReadA, ReadB}**

**Mealy Output Vector= {Reset, Inc\_Counter, Clr\_Counter, Accumulate, CalcResult\_ClrOperands}**

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**Submission details**

* **Your lab report, a .doc file, should contain properly commented Post-Lab task code, with Screenshots(of print preview) of Schematic and waveforms, and Critical Analysis.**
* **The report must have a title page in the pescribed format.**
* **Name the .doc file RegNo.docx; eg SP14-BCE-99.docx**
* **Sumbit on portal.**